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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09 892,713	06 28 2001	Yusuke Kohyama	01701.00090	4702

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EXAMINER

PHAM, LONG

ART UNIT PAPER NUMBER

2823

DATE MAILED: 09 06 2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/892,713

Applicant(s)

KOHYAMA, YUSUKE

Examiner

Long Pham

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) 5-18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 2 and 5 is/are rejected.
- 7) ☒ Claim(s) 3 and 4 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3, 4
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

**DETAILED ACTION**

***Election/Restrictions***

1. Applicant's election without traverse of claims 1-5 in Paper No. 6 is acknowledged.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Matsumoto (JA '221).

AAPA teaches a semiconductor device comprising (see figures 1A-1C and 2A-2C and the Background of the Invention on pages 1-8 of this application): capacitor structures, each having a first low electrode, a first insulating film formed on the first lower electrode and a first upper electrode formed on the first insulating film;  
electric fuse elements, each having a second lower electrode, a second insulating layer formed on the second lower electrode and a second upper electrode formed on the second insulating, the electric fuse having substantially same structure as that of the capacitor structures and being formed on the same level as that of the capacitor structures, wherein information is written in the electric fuse element depending on whether the second insulating film is dielectrically broken down, and a writing voltage of

the electric fuse is determined by dielectric breakdown resistance of the second insulating film.

AAPA further teaches that the capacitor structures require a high dielectric breakdown resistance or the first insulating layer has high dielectric breakdown resistance and that the electric fuse elements require a low dielectric breakdown resistance or the second insulating layer has a low dielectric breakdown resistance so that the fuse can be broken with lowest possible voltage but fails to teach that the second insulating layer has low dielectric breakdown resistance by having a higher impurity concentration than the first insulating layer as recited in present claim 1.

Matsumoto teaches that if the a gate oxide has higher impurity concentration, more breakdown is generated at low voltage or low dielectric breakdown resistance is obtained. See the English abstract.

It would have been obvious to **one of ordinary skill in the art of making semiconductor devices** to incorporate Matsumoto's teaching into the device of AAPA because in doing so the low dielectric breakdown resistance of the second insulating layer can be achieved. See The English abstract.

4. Claims 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Matsumoto (JA '221).

AAPA teaches a semiconductor device comprising (see figures 1A-1C and 2A-2C and the Background of the Invention on pages 1-8 of this application): capacitor structures, each having a first gate insulating layer film formed on a semiconductor substrate of a conductivity type, and a first gate electrode formed on the first gate insulating film; and electric fuse elements, each having a second gate insulating film formed on the semiconductor substrate and a second gate electrode formed on teh

second gate insulating film, wherein information is written in the electric fuse element depending on whether the second insulating film is dielectrically broken down, and a writing voltage of the electric fuse is determined by dielectric breakdown resistance of the second insulating film, wherein the first gate insulating film and the first gate electrode constitute a part of a MOS transistor.

AAPA further teaches that the capacitor structures require a high dielectric breakdown resistance or the first insulating layer has high dielectric breakdown resistance and that the electric fuse elements require a low dielectric breakdown resistance or the second insulating layer has a low dielectric breakdown resistance so that the fuse can be broken with lowest possible voltage but fails to teach that the second insulating layer has low dielectric breakdown resistance by having a higher impurity concentration than the first insulating layer as recited in present claim 2.

Matsumoto teaches that if the a gate oxide has higher impurity concentration, more breakdown is generated at low voltage or low dielectric breakdown resistance is obtained. See the English abstract.

It would have been obvious to **one of ordinary skill in the art of making semiconductor devices** to incorporate Matsumoto's teaching into the device of AAPA because in doing so the low dielectric breakdown resistance of the second insulating layer can be achieved. See The English abstract.

***Allowable Subject Matter***

5. Claims 3 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 703-308-1092. The examiner can normally be reached on M-F, 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-4082 for regular communications and 703-746-4082 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



Long Pham

Primary Examiner

Art Unit 2823

L. P.

September 3, 2002